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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,712	03/18/2004	Rafael Camarota	015114-069900US	7512

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,712	CAMAROTA ET AL.	
	Examiner	Art Unit	
	QUAN TRA	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-31 and 36-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,23-32,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/21/08 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 27, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fugate et al. (USP 6525594) in view of Tyckowski (USP 6359408) and Zhu et al. (USP 5933047).

Fugate et al.'s figure 2 shows an electronic system comprising: an integrated circuit comprising: an output buffer comprising a pull-up transistor (22) coupled between a pad (at Vo) and a first supply voltage; and a switch 32 coupled to the bulk of transistor 22, a hot-socket circuit (34) coupled to the pad and the first supply voltage, wherein the hot-socket circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage. Figure 2 fails to show a logic circuit coupled to the output of the hot-socket. However, Tyckowski's figure 1 shows a logic circuit 29 coupled to the output of comparator circuit 27 in

order to allow or prevent the output of the comparator controlling circuit 30. Therefore, it would have been obvious to one having ordinary skill in the art to add Tyckowski's logic gate 29 to couple to the output of Fugate et al.'s comparator 34 for the purpose of disabling the switching function when not needed. It is also seen as an obvious design preference to select the bulk of Fugate's transistor 22 to connect to Vdd when the logic circuit is enable dependent upon a particular environment to ensure optimum performance, see Fugate's figure 1. Figure 2 further show that when the enable signal is in a disable state, the bulk of the pullup device is coupled to the higher voltage of the pad or the first supply voltage. Fugate et al.'s figure 2 further fails to show the detail of the switch 32. However, Zhu et al.'s figure 4 shows an integrated switch circuit (P3, P4, 102). It would have been obvious to one having ordinary skill in the art to use Zhu et al.'s integrated switch circuit for Fugate et al.'s switch 32 for the purpose of saving space. Thus, the modified Fugate et al.'s figure 2 further shows a first transistor (Zhu's P3) coupled between a bulk of the pull-up transistor and a source of the pullup transistor, and having a gate coupled to receive a control signal (output of 34); and a second transistor (Zhu'P4) coupled between a drain of the pullup transistor and the bulk of the pull-up transistor, and having a gate coupled to receive a complement of the control signal; wherein when the control signal is in a first state, the bulk of the pull-up transistor is coupled to the pad and when the control signal is in a second state, the bulk of the pull-up transistor is couple to the first supply voltage; and a drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad.

As to claim 39, the modified Fugate et al.'s figure 2 shows an integrated circuit comprising: a pull-up MOS transistor (22) coupled between a pad and a first supply voltage; a pull-down MOS transistor (24) coupled between the pad and a second supply voltage that is lower than the first supply voltage; a first MOS transistor switch (Zhu's P3 that is used in Fugate's 32) having a source/drain terminal coupled to the first supply voltage; a second MOS

transistor switch (Zhu's P4 in Fugate's 32) coupled between the first MOS transistor switch and the pad, the second MOS transistor switch having a bulk terminal coupled to the bulk terminal of the first MOS transistor switch and a common source/drain terminal of the first and second MOS transistor switches; a comparator circuit (34) coupled to the pad and the first supply voltage, wherein the comparator circuit provides an output having a first state if a voltage on the pad is higher than the first supply voltage and a second state if the voltage on the pad is lower than the first supply voltage; and a first logic block (the added AND gate) configured to perform logical AND operation and responsive to output signal of the comparator circuit and an enable signal; and a second logic block (Zhu's 102) configured to perform logical inversion operation and responsive to the first logic block, the second logic block disposed between gate terminals of the first and the second MOS transistor switches

As to claim 40, Fugate's figure 2 shows a first predriver circuit (8) coupled to a gate terminal of the pull-up MOS transistor; and a second predriver circuit (9) coupled to a gate terminal of the pull-down MOS transistor.

3. Claims 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al. (USP 5514893) in view of Verhaege et al. (USP 6529359), Djakovic (USP 6351539), Fugate et al. (USP 6525594), Tyckowski (USP 6359408) and Zhu et al. (USP 5933047).

As to claim 26, 28 and 29, the combination of Miyanaga et al., Verhaege et al, and Djakovic (USP 6351539) (see previous rejection of claim 1) shows all elements of the claim except for a switch circuit coupled to the bulk of the pull-up transistor. However, the combination of Fugate et al., Tyckowski, and Zhu et al. (see the rejection of claim 27) shows a circuit having switch circuit (the modified 32 and 34) coupled to the bulk of pull-up transistor 22 in order to prevent sudden voltage drop at the bulk, thereby reducing output noise. Therefore, it

would have been obvious to one having ordinary skill in the art to add the modified Zhu et al.'s switch circuit to Miyanaga et al.'s pull-up transistor 4 for the purpose of reducing output noise.

As to claim 30, the combination of the above references shows that the logic circuit is an AND gate.

As to claim 31, the combination of the above references fails to teach plurality of programmable logic elements. However, it would have been obvious to one having ordinary skill in the art to use the modified Miyanaga et al.'s circuit in a circuit comprising programmable logic elements in order to take advantage of the modified Miyanaga's benefit to the programmable logic elements circuit.

4. Claims 36-38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyanaga et al.'s (USP 5514893) in view of Toyoshima (US 20010017755), Lin (USP 6552594) and Fugate et al. (USP 6525549).

As to claim 36, Miyanaga et al.'s figure 1 shows an integrated circuit comprising: a pull-up MOS transistor (4) coupled between a first supply voltage and a pad; a pull-down MOS transistor (5) coupled between the pad and a second supply voltage that is lower than the first supply voltage; an active diode (2) having a second terminal coupled to the pad. Figure 1 fails to show a switch transistor coupled between the diode and the first supply voltage. However, Toyoshima's figure 2 shows diode D1 and switch F1 are coupled between pad 10 and Vcc in order to provide a controllable clamp circuit, and Lin's figures 11a and figures 11b show the function of the diode in circuit 60 will not be changed when the positions of switch P1 and the diode are exchange. Therefore, it would have been obvious to one having ordinary skill in the art to add a PMOS switch (i.e. Lin's transistor P1) connected between Miyanaga's diode 2 and the first supply voltage for the purpose of having more flexibility of enabling/disabling the clamp

diode 2. The modified Miyanaga et al.'s figure 1 further fails to show "a biasing circuit adapted to apply to bulk regions of the pull-up MOS transistor and the first MOS transistor switch the higher of a voltage applied to the pad and the first supply voltage". However, Fugate et al.'s 2 teaches that a bulk of PMOS transistor is selectively coupled to the highest voltage in order to prevent sudden voltage drop at the bulk, thereby reducing output noise. Therefore, it would have been obvious to one having ordinary skill in the art to use Fugate et al.'s bias circuit to bias the bulks of the pull-up MOS transistor (4) and the added PMOS switch in order to reduce output noise and power consumption.

As to claim 37, the modified Miyanaga et al.'s figure 1 further shows an input buffer (6, 7) coupled directly to the pad.

As to claim 38, the modified Miyanaga et al.'s figure 1 further shows a first predriver (8) circuit coupled to a gate terminal of the pull-up MOS transistor; and a second predriver circuit (9) coupled to a gate terminal of the pull-down MOS transistor.

As to claim 41, Miyanaga et al.'s figure 1 further shows a resistor (6) external to the integrated circuit.

Response to Arguments

5. Applicant's arguments have been fully considered but they are not persuasive.

Applicant argues that there is no disclosure, whatsoever, in Tyckowski of a "logic block" that can "provide the control signal" that when placed "in a second state" can cause "drain-to-bulk diode of the pull-up transistor clamps a voltage received at the pad". However, the combination of Fugate and Tychoswki shows a logic block (the added AND gate) provide the control signal that when placed in a second state can cause drain-to-bulk diode of the pull-up

transistor clamps a voltage received at the pad. When the bulk of Fugate's transistor 22 the pn junction between the drain and the bulk of transistor 22 will clamp the output node vo.

Applicant further argues that there is no motivation to combine Fugate with Tyckowski. However, Tyckowski used the AND gate to enable/disable the output of comparator circuit. Therefore, one skilled in the art would have motivated to use AND gate to enable/disable the output of Fugate's comparator in order to have more flexibility of controlling the bulk bias voltage. The intended function of Fugate will not be changed when adding the AND gate but would have more flexibility of controlling the bulk bias voltage.

Applicant further argues that Fugate, even when taken in combination with Tyckowski and Zhu fails to teach or suggest "a logic circuit coupled to receive the output of the hot-socket circuit and an enable signal and to provide the control signal, wherein when the control signal is in a first state, the bulk of the pull-up transistor is coupled to the pad…The Examiner respectfully disagrees. N new ground rejection is introduced as necessitated by amendment. Furthermore, any "state" can be considered as "disable state" or "enable state".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to QUAN TRA whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/QUAN TRA/
Primary Examiner, Art Unit 2816